

**OptiMOS<sup>®</sup> 3 Power-Transistor**
**Features**

- MOSFET for ORing and Uninterruptible Power Supply
- Qualified according to JEDEC<sup>1)</sup> for target applications
- N-channel
- Logic level
- Ultra-low on-resistance  $R_{DS(on)}$
- 100% Avalanche tested
- Pb-free plating; RoHS compliant

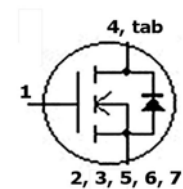
**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	0.95	m $\Omega$
$I_D$	180	A

PG-TO263-7



Type	Package	Marking
IPB009N03L G	PG-TO263-7	009N03L


**Maximum ratings, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ }^\circ\text{C}$	180	A
		$V_{GS}=10\text{ V}, T_C=100\text{ }^\circ\text{C}$	180	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ }^\circ\text{C}$	180	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ }^\circ\text{C}$	180	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ }^\circ\text{C}$	1260	
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	$T_C=25\text{ }^\circ\text{C}$	100	
Avalanche energy, single pulse	$E_{AS}$	$I_D=100\text{ A}, R_{GS}=25\text{ }\Omega$	610	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=180\text{ A}, V_{DS}=24\text{ V}, di/dt=200\text{ A}/\mu\text{s}, T_{j,max}=175\text{ }^\circ\text{C}$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$		$\pm 20$	V

<sup>1)</sup> J-STD20 and JESD22

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	250	W
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	0.6	K/W
SMD version, device on PCB	$R_{\text{thJA}}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>4)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\text{ }\mu\text{A}$	1	-	2.2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	2	$\mu\text{A}$
		$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	20	200	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=100\text{ A}$	-	0.95	1.3	$\text{m}\Omega$
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=100\text{ A}$	-	0.7	0.95	
Gate resistance	$R_{\text{G}}$		-	1.5	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=100\text{ A}$	180	370	-	S

<sup>2)</sup> See figure 3 for more detailed information

<sup>3)</sup> See figure 13 for more detailed information

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	19000	25000	pF
Output capacitance	$C_{oss}$		-	5700	7600	
Reverse transfer capacitance	$C_{rss}$		-	360	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=1.6\ \Omega$	-	26	-	ns
Rise time	$t_r$		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	103	-	
Fall time	$t_f$		-	22	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	50	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	28	-	
Gate to drain charge	$Q_{gd}$		-	24	-	
Switching charge	$Q_{sw}$		-	46	-	
Gate charge total	$Q_g$		-	110	146	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	V
Gate charge total	$Q_g$	$V_{DD}=15\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	227	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	95	-	
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	148	-	

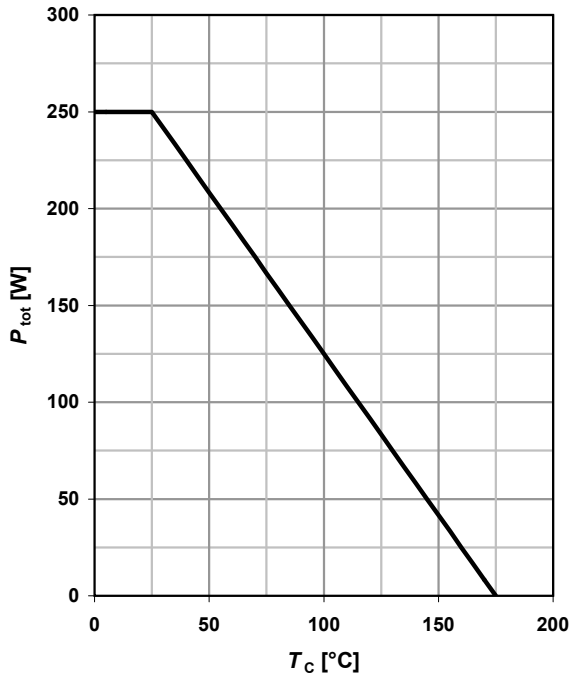
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	180	A
Diode pulse current	$I_{S,pulse}$		-	-	1260	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.82	1	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	135	-	nC

<sup>5)</sup> See figure 16 for gate charge parameter definition

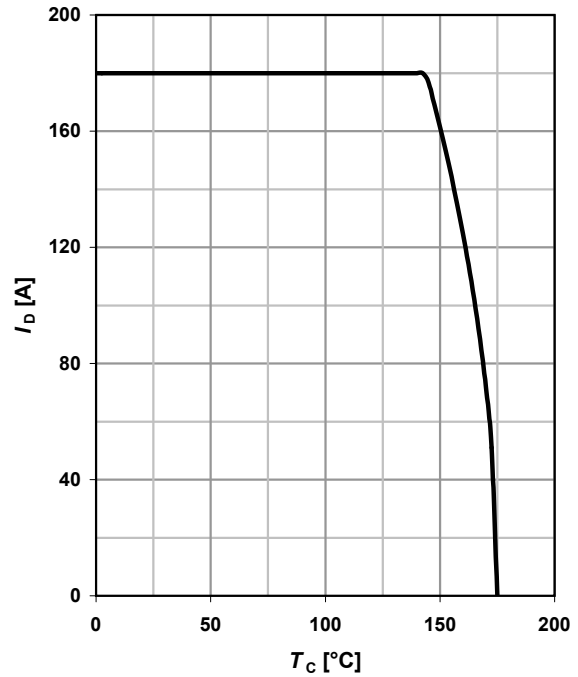
**1 Power dissipation**

$$P_{tot} = f(T_C)$$



**2 Drain current**

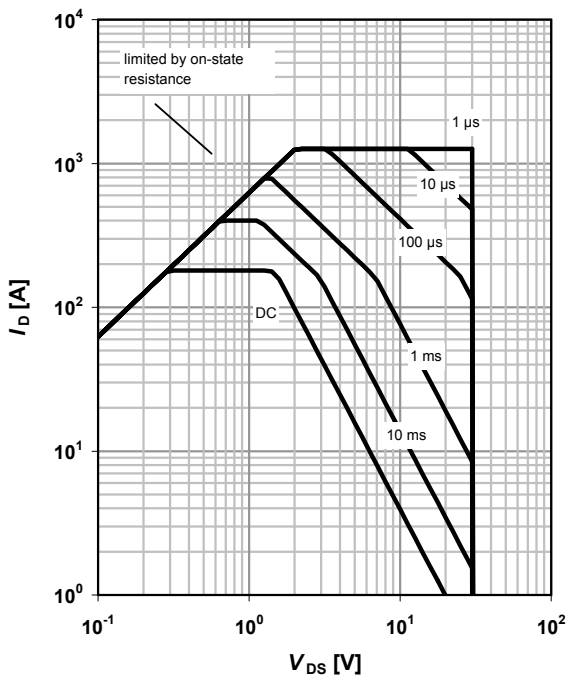
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

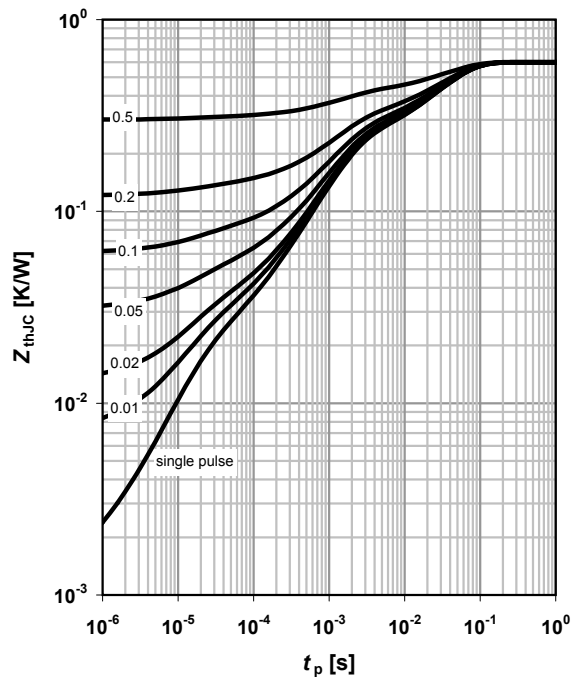
parameter:  $t_p$



**4 Max. transient thermal impedance**

$$Z_{thJC} = f(t_p)$$

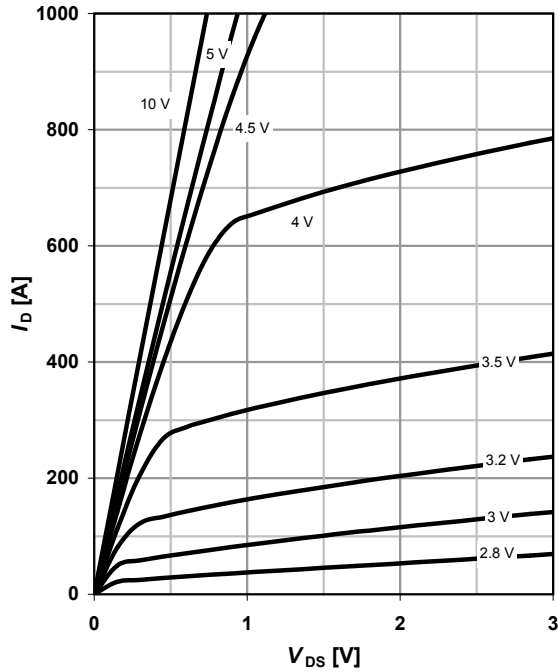
parameter:  $D = t_p / T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

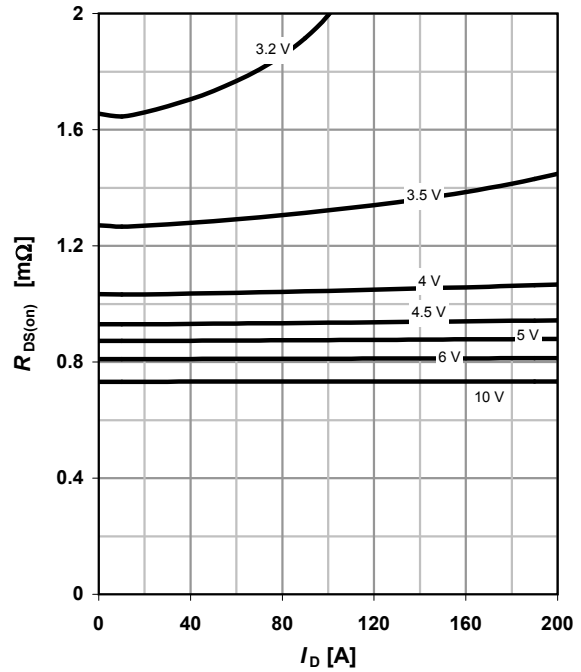
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

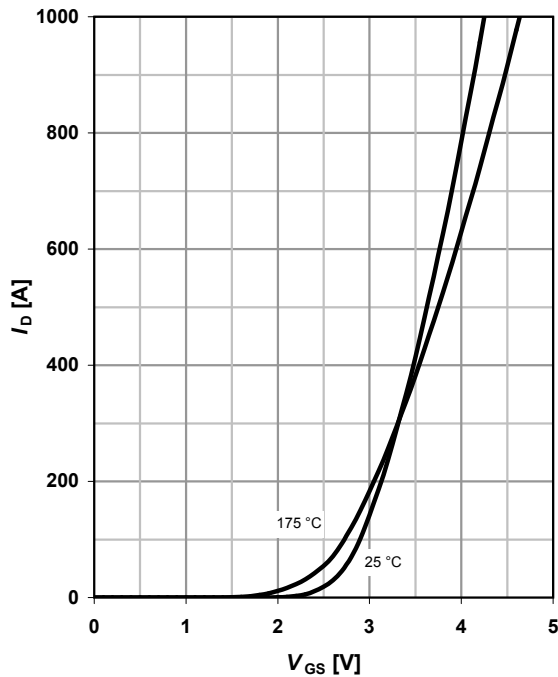
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

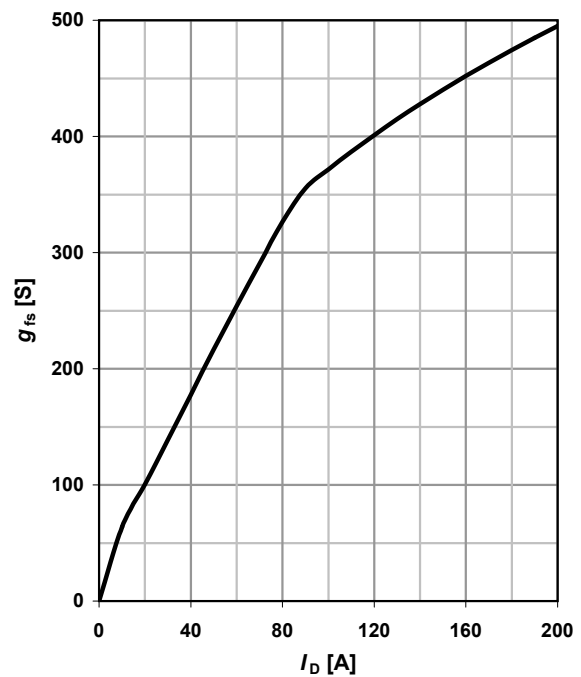
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



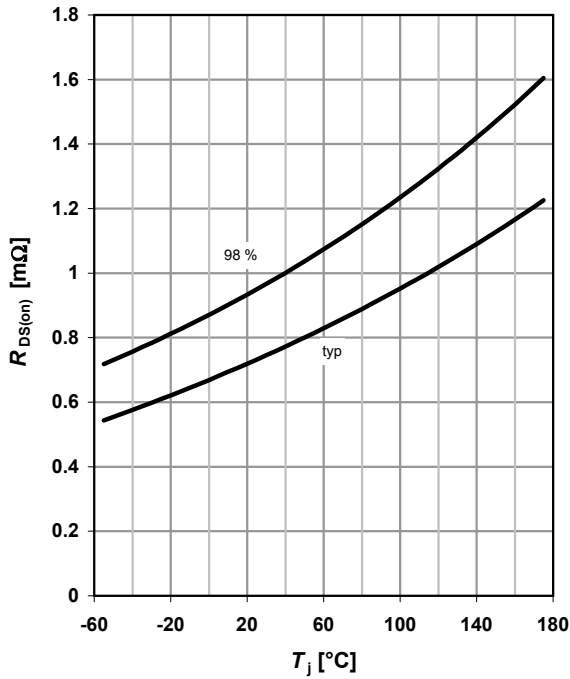
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



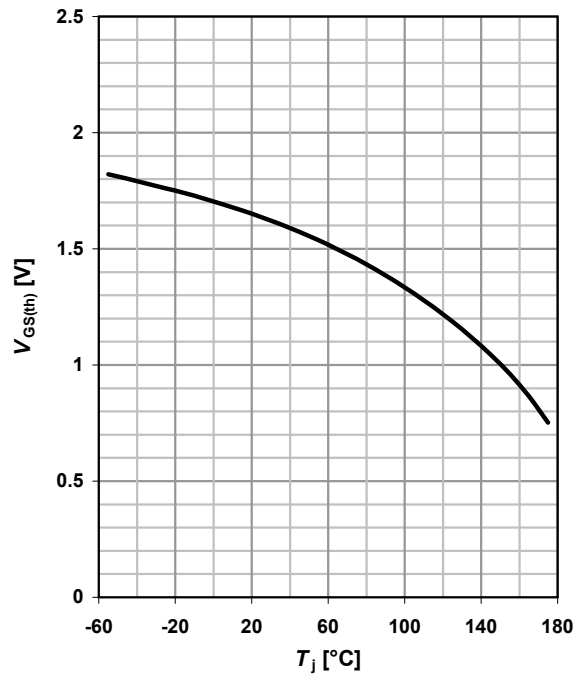
**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j); I_D = 100 \text{ A}; V_{GS} = 10 \text{ V}$



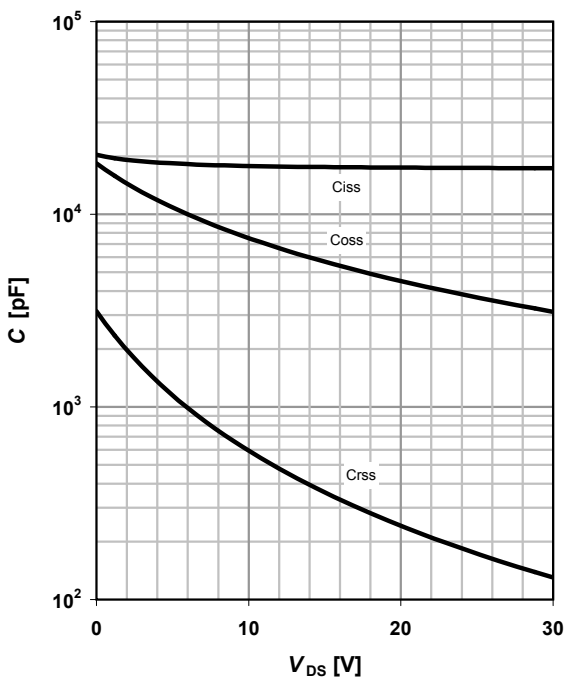
**10 Typ. gate threshold voltage**

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 1 \text{ mA}$



**11 Typ. capacitances**

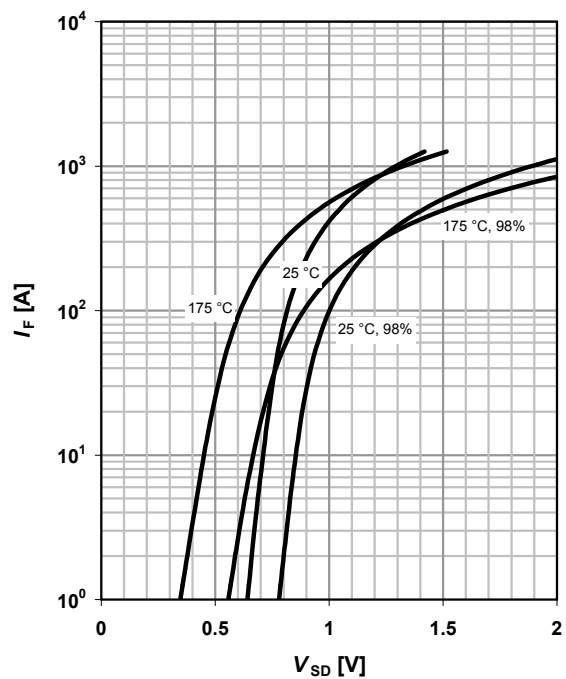
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

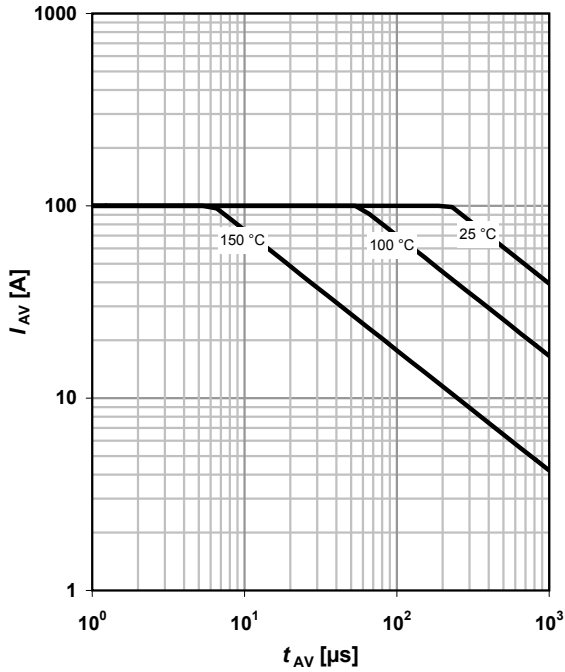
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

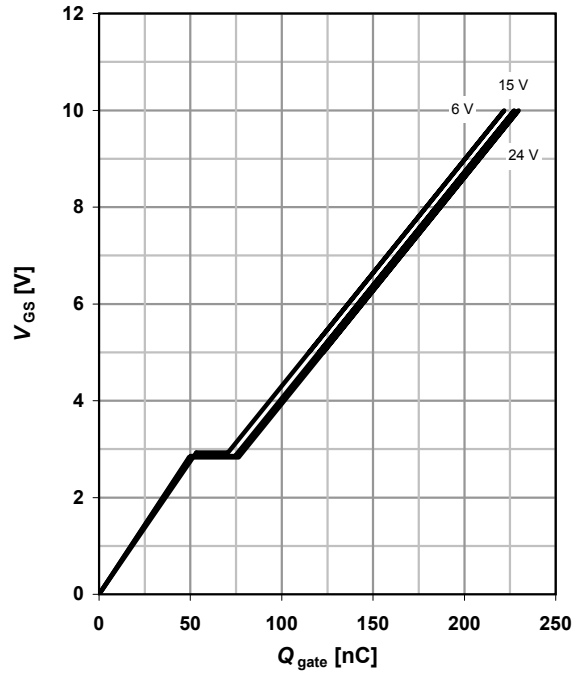
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

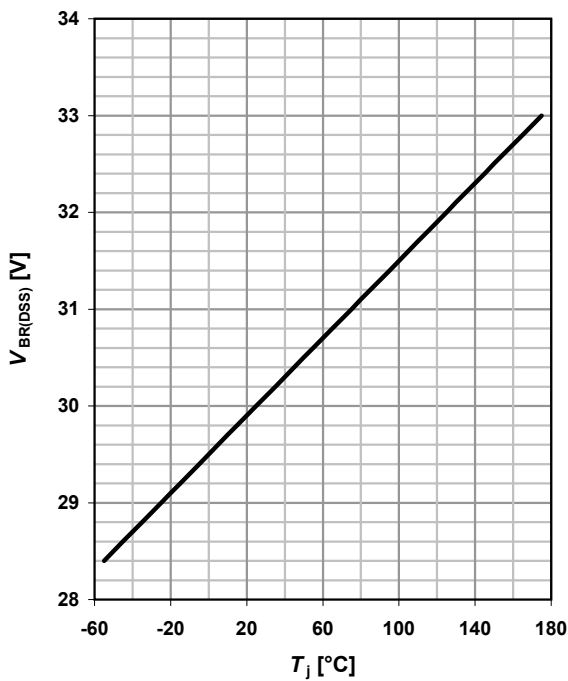
$V_{GS}=f(Q_{gate}); I_D=100 \text{ A pulsed}$

parameter:  $V_{DD}$



**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

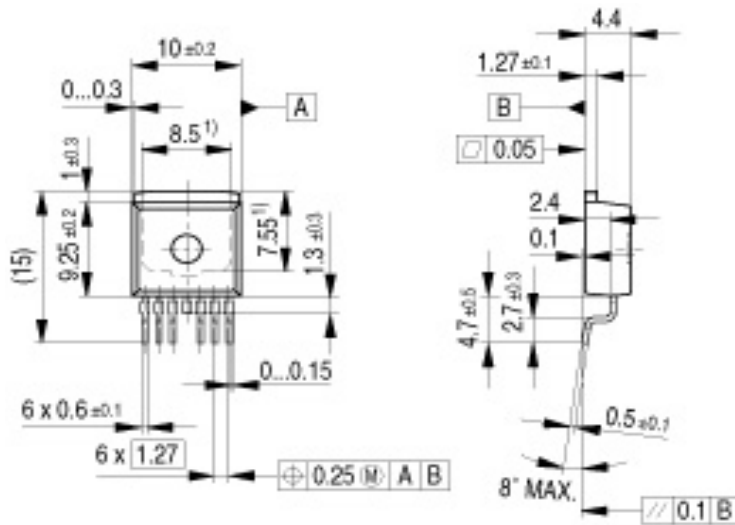


**16 Gate charge waveforms**



Package Outline

PG-TO263-7



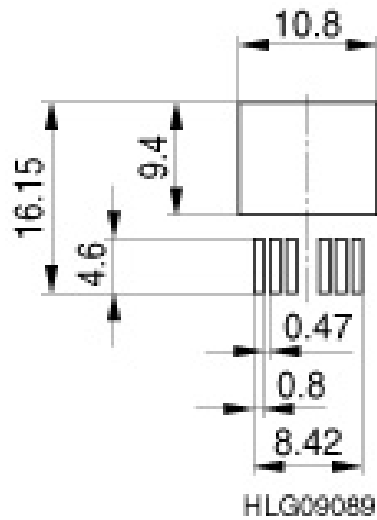
1) Typical

Metal surface min. X = 7.25, Y = 6.9

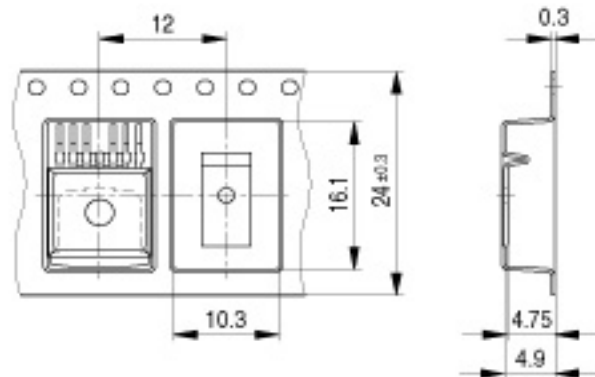
All metal surfaces tin plated, except area of cut.

GPT09003

Footprint:



Packaging:





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